

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination PEREZ ET AL.	
		Examiner Nghia M. Doan	Art Unit 2825	Page 1 of 1

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**NON-PATENT DOCUMENTS**

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U	Quincke J., Novel test structure for the investigation of the efficiency of guard ring used for I/O latch-up prevention, March 1990, Vol. 3, pages 35-39.		
V	Ker et al., Automatic methodology for placing the guard ring into chip layout to prevent latch-up in CMOS IC's, Sept 2001, Vol. 1, pages 113-116.		
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.